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The Noise and Suppression Transfer Functions of the Anti-Jitter Circuit.

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***Abstract* – The Anti-Jitter Circuit suppresses the phase and time jitter on a frequency source by feed-forward cancellation automatically balanced over a wide range of source frequencies. The balance is maintained by a 'DC-Removal' feedback control loop that results in a lowest base-band (or sideband) jitter suppression frequency for the AJC and a consequential limitation on the final settling speed for the phase error. In this paper an 'Analytic AJC System Simulator', written in Mathcad is used to find some 'optimum' sets of AJC control loop parameters. The AJC transfer functions for 'jitter suppression' and for the filtering of the two main noise sources, 'integrator noise' and 'comparator noise', are derived from the AJC system block diagram. Then for typical values of the two noise sources the total predicted output noise spectrum and the suppression ratio are plotted in a format suitable for comparison with measured noise and suppression results from a spectrum analyser. By integration of the predicted noise spectra the Mathcad simulator also can produce estimates for the total jitter limit of the AJC internally generated noise. These confirm that the AJC close-to-carrier noise (inside the loop bandwidth) is much less than for a typical PLL of the same bandwidth (because there is no division in the AJC). For an AJC (discharge) current of 1mA the further out sideband noise corresponds to a VCO with a Q of about 5 to 10; with an increase of equivalent Q to 50 to 100 if the discharge current is raised to 10mA.**

***Keywords* – Time jitter, phase noise, AJC, jitter suppression technology, system simulator, total time jitter.**

I. INTRODUCTION

The Anti-Jitter Circuit (AJC) was announced at the EFTF in 1996 [1] and it has undergone progressive improvement since then [2,3,4,5,6]. Discrete component AJCs are now available (from Toric Limited) which at 40 MHz give 20-40dB suppression of wideband phase noise and time jitter, and operate up to 150MHz, still with some suppression. The noise performance, particularly at lower sideband frequencies, is demonstrably improved over a comparable RC oscillator with or without an associated phase-locked loop (PLL). A collaborative development programme, operating under the pan-European 'Eureka' programme, is now running (and is open to new participants). It is aimed at solving the problems of implementing this new technology in integrated circuit form. The 14th EFTF paper given in Torino [6] gave a first analysis of Shot noise in the AJC. Later analysis, however, showed that Shot noise was not particularly significant. The choice of a suitably low noise transistor and suitable feedback for the key current source in the AJC removed this supposed problem. In fact we find the noise sources in the AJC are well represented by assuming a noise figure for the AJC comparator no larger than normal. Also the 14th EFTF paper did not give general expressions for the AJC noise and suppression transfer functions and so this is now presented in this paper.

The AJC suppresses phase noise and time jitter on any input signal by a feed-forward cancellation process. The process is self-adjusting so that as the frequency is changed the degree of cancellation and noise suppression is maintained. However the AJC always has a lower frequency limit for noise and jitter suppression. This limit and the associated settling time after a frequency or phase step, is determined by the integrator time constant and the feedback gain and time constants. Feedback has to be applied to maintain correct AJC operation as the input frequency is changed; often over a 10:1 frequency range or more. A circuit designer must make a selection from a range of possibilities for the loop transfer function, and so a method is needed to find the best choice.

A novel Analytic AJC System Simulator has been written (for Toric Limited) as a Mathcad worksheet. This simulator performs an analysis of any AJC system simultaneously in terms of its root locus, closed- and open-loop transfer functions, and frequency and time responses. Graphical outputs are arranged to mimic what can be seen on a spectrum analyser and on an oscilloscope. Outputs respond to parameter changes in about a second, making it a most useful AJC design tool. There is a companion PLL simulator allowing the AJC and a PLL to be compared directly when appropriate. The simulator represents the noise and suppression transfer functions of any chosen AJC configuration directly in the graphical outputs. Total time jitter estimates are also available from the simulator.

II BASIC PRINCIPLES OF THE AJC

Phase noise and time jitter are predominantly carried in the waveform transitions or zero crossings of any frequency source input. The AJC removes jitter in these transitions.

The AJC measures the jitter at the start of each clock cycle by comparing it with the long term average of the jitter of an input signal and half a cycle later creates a new output clock transition where the original jitter has been substantially cancelled. Fig 1 shows how this is done.

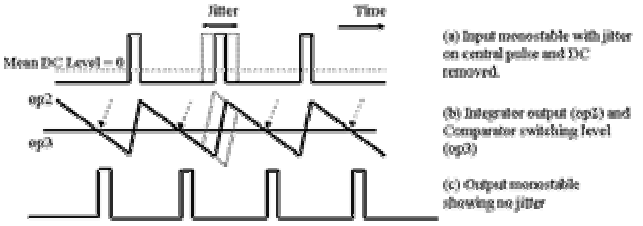

Fig.1. AJC timing diagram.

AJC Basic Principles for Fig.1.-

The integrator converts the input pulse train into a sawtooth waveform with a constant or zero mean DC level, with no 'drift' up or down.

The comparator switching level op3 is constant, usually chosen to be near the mean sawtooth level.

Time jitter on any input pulse does not affect the time of intersection of the slow (downslope) ramp of the integrator waveform op2 with the comparator switching level op3.

The output monostable, triggered from this intersection, has much reduced time jitter and phase noise.

The (mark) pulse length of the output monostable can be chosen to be half a period (equal mark-space ratio).

The lowest sideband frequency of jitter or phase noise suppression is the DC removal cut-off frequency.

The input monostable pulse DC is removed by AC coupling, or by DC feedback around the integrator.

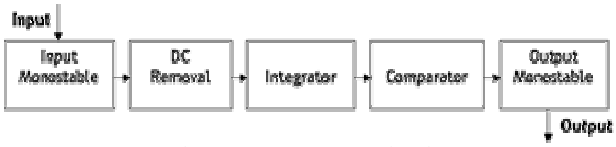

Fig. 2. AJC processes or functions

As shown in Fig, 2 there are *five 'functions'* or *processes* in an AJC :-

1) Formation of a pulse train of constant area input pulses- from the input monostable or a pulse forming network.

2) DC removal by feedforward, feedback, AC coupling, or by a combination of these.

3) Integration of the (input) pulse train to give a sawtooth waveform. (The DC removal process ensures that this does not "drift" up or down).

4) Comparator Switching at approximately the mean level of the sawtooth waveform.

5) Formation of new output pulses of chosen length triggered from a fixed (mean) level on the integrator sawtooth low jitter (down) slope.

In Fig,3 the five AJC functions can be seen to apply in the basic 'Adiabatic AJC' [4]. This figure shows that the adiabatic central core performs the first three functions and part of the fourth (comparator) function. The adiabatic AJC as shown illustrates the simplicity of the AJC concept.

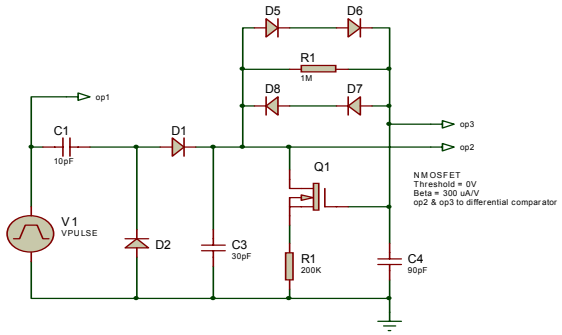

Fig. 3. Basic Adiabatic AJC core

A.. AJC Performance Specifications

The key factors defining AJC performance are:-

1) AJC Suppression in dB as a function of the upper and lower sideband frequencies.

2) AJC Operating Frequency Range from highest to lowest frequency without external adjustment or change of components.

3) AJC Locking and Settling Speed after a frequency or phase jump.

4) Intrinsic AJC Noise - This is the limiting level and spectrum of the internal or intrinsic noise as it appears at the AJC output.

5) Total Jitter using a measure appropriate to the application.

VI. MEASUREMENT OF AJC PERFORMANCE

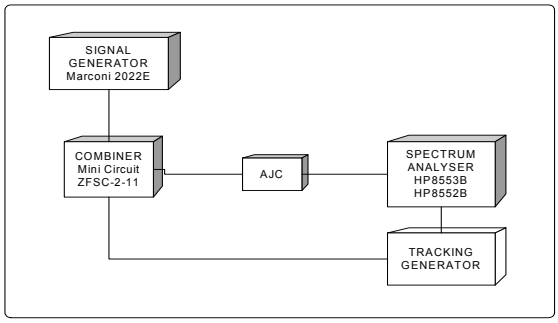

Fig. 4. 'Huddart' AJC performance measurement method

The David Huddart method for measuring and displaying AJC suppression and internal noise as a function of sideband frequency is shown in Fig. 5. Note that the results shown throughout this paper were obtained using the more modern HP8642A signal generator and HP8650A spectrum analyser.

To measure AJC Suppression:-

The signal from the tracking generator is first set to be 20db below the signal source (with the AJC by-passed). If desired a -20dB reference level can be stored on the spectrum analyser as

shown in Fig. 5. Suppression is measured relative to this level, (but subtracting 0 to 6dB to account for the AJC input stage clipping and limiting the input signal). Note that in Fig. 5 an under-damped AJC loop can cause 'negative' suppression at the loop cut-off frequency.

To measure AJC internal or 'intrinsic' noise:-

The tracking generator is switched off

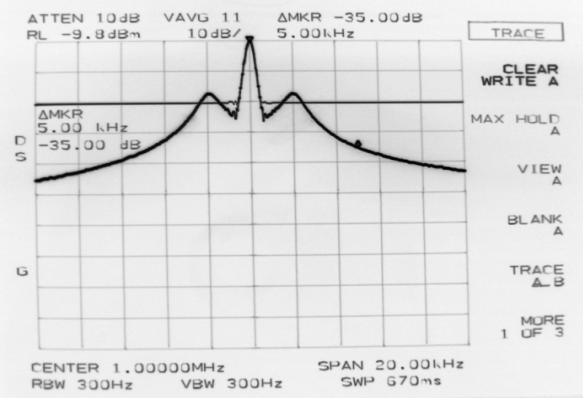

Fig. 5. Suppression of 1MHz AJC

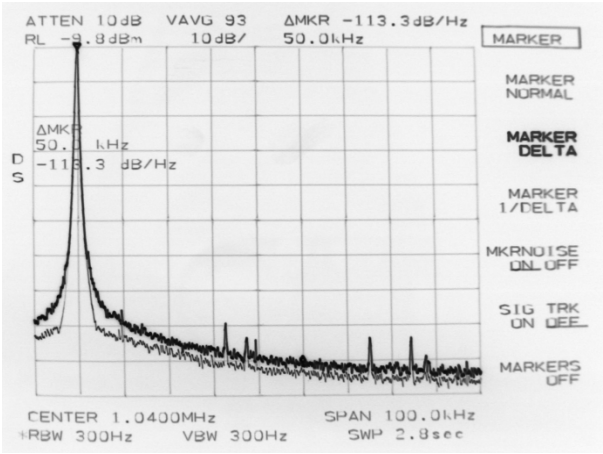

Fig. 6. Measurement of 1MHz AJC internal or 'intrinsic' noise

III TIME JITTER DEFINITION

Total Jitter Measurement

Jitter can be seen on the time waveform transitions on oscilloscope or on the transitions in an 'eye diagram'. The amount of jitter seen depends on the level, the jitter spectrum shape, and the 'delayed' triggering point on the waveform.

A relatively new but useful practice is to normalise the time jitter with respect to one period or Unit Interval ('UI' = one period of the input frequency). For a Gaussian distribution of the transitions around a mean transition position the standard deviation is taken to be the total or rms jitter level.

Ideally time jitter should be measured relative to a 'clean' clock that has no jitter. The clock has to be set to exactly the mean frequency of the jitter wave form. In this way we can measure 'absolute' or unweighted time jitter.

It is difficult to make a 'clean' clock that covers a wide frequency range and so 'jitter analysers' measure the exact time differences between pairs of waveform transitions a time τ apart. The lowest jitter frequency that can then be measured accurately is the reciprocal of τ. For 'wander', which is very low frequency jitter, τ has to be very long. All jitter analysers are limited in this respect.

Two measurements τ apart and subtracted correspond to a filter with a power transfer function of $\mathrm{Sin}^2(2\pi f\tau)$ This has a notch at zero frequency and thereafter for every multiple of $f = 1/2\tau$. A combination of pairs of measurements can remove all notches except the one at zero frequency, but at the cost of a small amount of widening of this notch.

In theory it is easy to compute the total time jitter from any measured or computed jitter spectrum. It is the integral of the Power Spectral Density of the spectrum over a given frequency range. In practice this is only meaningful if upper and lower frequency limits are set for this. The upper frequency limit is usually taken to be the carrier frequency of the source itself. The lowest 'sensible' frequency limit is set by the system requirements of the chosen system application.

For example in 'self-clocking' systems where a clock is extracted from the (data) signal itself, there will always be a longest response time and hence highest low frequency jitter frequency f_l that can be tolerated. There is no point in measuring jitter at lower frequencies than this. With the AJC it is possible to choose the lowest suppression frequency and intrinsic noise band width to optimise the total jitter performance for the required overall system lower frequency limit.

The total jitter in UI (Unit Interval) units for a spectrum $L(f)$ from low frequency a to high frequency b is

$$UI = \tau_{tot}/T_0 = (f_0/\pi)\sqrt{\left[\int_a^b L(f)\,df\right]} \qquad (1)$$

and $T_0 = 1/f_0$ is the period of the carrier f_0 . The default value for b is the carrier frequency f_0. (As a reminder, $L(f)$ is the phase noise sidebands as seen on a spectrum analyser.)

For *AJC internal noise* we can take b as zero and get an integral that always converges. This is what is used in the A2S2 to estimate the 'intrinsic jitter' of the AJC (i.e. $a = 0$ and $b = f_0$).

A total jitter measure gaining currency is the cycle-to-cycle time jitter. A cycle-to-cycle jitter measurement corresponds to a $Sin^2(2\pi f/f_0)$ band-pass filter being applied to the jitter power spectrum. This filter has notches at DC and at the carrier frequency and harmonics of this. For an oscillator spectrum with any plateau noise subtracted, this has a meaningful constant value.

A known jitter spectrum including any discrete components can be plotted appropriately as a simple log $L(f)$, $\log f$ or $\log \tau$ graph to give the total time jitter between any two frequency or measurement time limits.

The planned version of the A2S2 will be able to compute the absolute and cycle-to-cycle total jitter UI figures for any AJC plus given oscillator spectrum combination.

IV SUPPRESSION AND NOISE TRANSFER FUNCTIONS

Jn Fig. 7, the block diagram of the AJC as a control system **the main blocks** are:-

1) Comparator Gain $k_c = V_{cc} / V_{pp}$ where V_{cc} is the comparator output voltage swing and V_{pp} is the peak to peak voltage swing of the integrator sawtooth

2) Integrator gain $k_i = g_m R_i$, where R_i is the (equivalent) integrator (ac) resistance across the integrator capacitor and g_m is the transconductance of the integrator discharge transistor.

3) Integrator cut-off (the main system pole), where C_i is the integrator capacitor , is given by:-

$$G_{ic}(s) = 1/(s R_i C_i + 1) = 1/(s + b) \quad (2)$$

4) Comparator dc feedback $G_c(s)$ is a control loop low-pass filter. This form of feedback ensures that the comparator always switches. If present, $G_c(s)$ will have one significant pole and also it can usefully have a have a left-hand-plane pole or right-hand-plane zero.

5) Mean dc feedback $k_d G_d(s)$. This is a more stable form of dc removal feedback. (But $k_d = 0$ in the following examples.)

The Transfer Functions :

1) Typically the loop transfer function has one pole, or two poles with a zero. A RHP zero can be created if positive ac feedback is used. (This is a very useful option.)

2) Transfer function from N_i to output (with $k_d = 0$):

$$G_{ni}(s) = G_{ic}(s) /\{ 1 + k_r\ k_c\ k_i\ G_c(s)\ G_{ic}(s)\} \quad (3)$$

3) Transfer function from comparator input noise N to output (with $k_d = 0$):

$$G_{nc}(s) = 1 /\{ 1 + k_r\ k_c\ k_i\ G_c(s)\ G_{ic}(s)\} \quad (4)$$

4) Suppression transfer function (with $k_d = 0$):

$$G_h(s) = 1 - k_r /\{ 1 + k_r\ k_c\ k_i\ G_c(s)\ G_{ic}(s)\ \} \quad (5)$$

5) An example of suppression transfer function for a second order system with two equal poles is

$$G_h(s) = k_a^2 / \{ (s+a)^2 + k_a^2 \} \quad (6)$$

Intrinsic Noise:-

1) Integrator resistor noise $N_i = 4kTR_i$ and $kT = 4 \times 10^{-21}$ watt/Hz. $R_i = 2.5$M gives close-in plateau noise of -140dBc/Hz if the sawtooth has an amplitude of $V_{pp} = 1$.

2) Above the loop bandwidth integrator noise is reduced by at least 6db/octave.

3) This gives a predicted AJC performance equivalent to a typical PLL frequency synthesiser VCO (with a $Q = 50$ to 100).

4) Noise N_c from comparator input: A value of N_c = 10nV/√Hz gives plateau noise beyond the 'noise shoulder' at the loop cut-off frequency of -150dBc/Hz if $V_{pp} = 1$.

5) It should be possible to reduce comparator noise to N_c = 1nV/√Hz with better input devices. This would give a plateau noise of -170dBc/Hz !

6) Note that (in theory) these noise sources are independent of input signal (carrier) frequency, provided that the integrator capacitor C_i is kept constant. In practice as the frequency is increased the discharge current increases in proportion and so C_i has to reduce to keep it to the typical 1ma level.

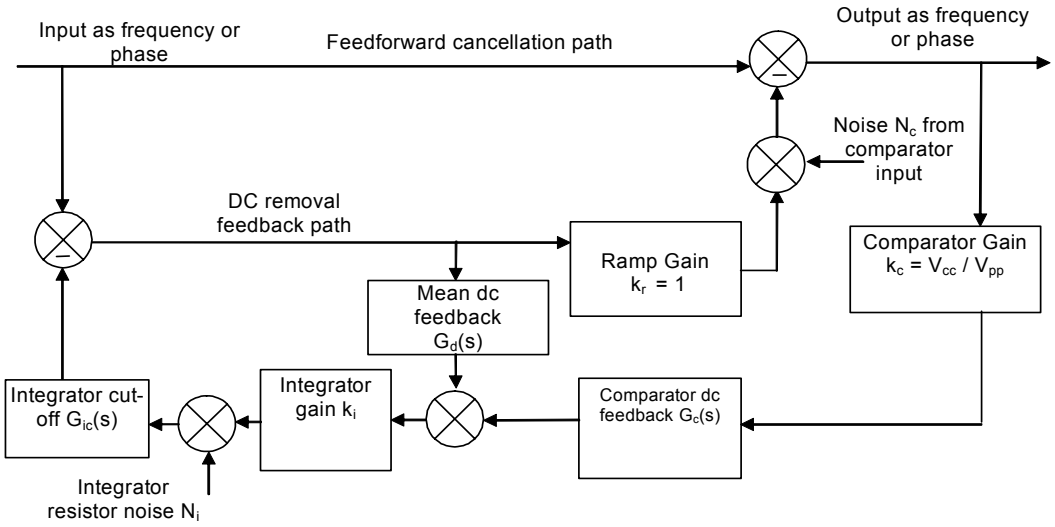

Fig. 7. Block diagram of AJC noise and suppression transfer functions

V ANALYTIC AJC SYSTEM SIMULATOR AND RESULTS

A system designer has to choose a suitable loop transfer function for the envisaged application, and so a method is needed to find the best choice.

A novel Analytic AJC System Simulator has been written (for Toric Limited) as a Mathcad worksheet. It analyses any AJC system simultaneously in terms of its open- and closed-loop transfer functions and gives as outputs:-

1) root locus,
2) loop time response (as seen on an oscilloscope).
3) frequency responses (as seen on a spectrum analyser), for (a) AJC suppression, (b) input signal spectrum (assumed), and (c) input spectrum after suppression,

4) Suppressed comparator noise
5) Suppressed integrator noise

Outputs respond to parameter changes in about a second, making it a most useful AJC design tool.

There is a companion PLL simulator allowing the AJC and a PLL to be compared directly when appropriate.

Typical graphical outputs can be seen in Figs. 8 to 11.

Total time jitter estimates can be automatically calculated.

Four representative examples of AJC control systems are now given. Figs. 8 to 11 for each system example give the root locus and time reponse at the top. The bottom left plots are for a noisy oscillator input and the bottom right plots are for a low noise oscillator input.

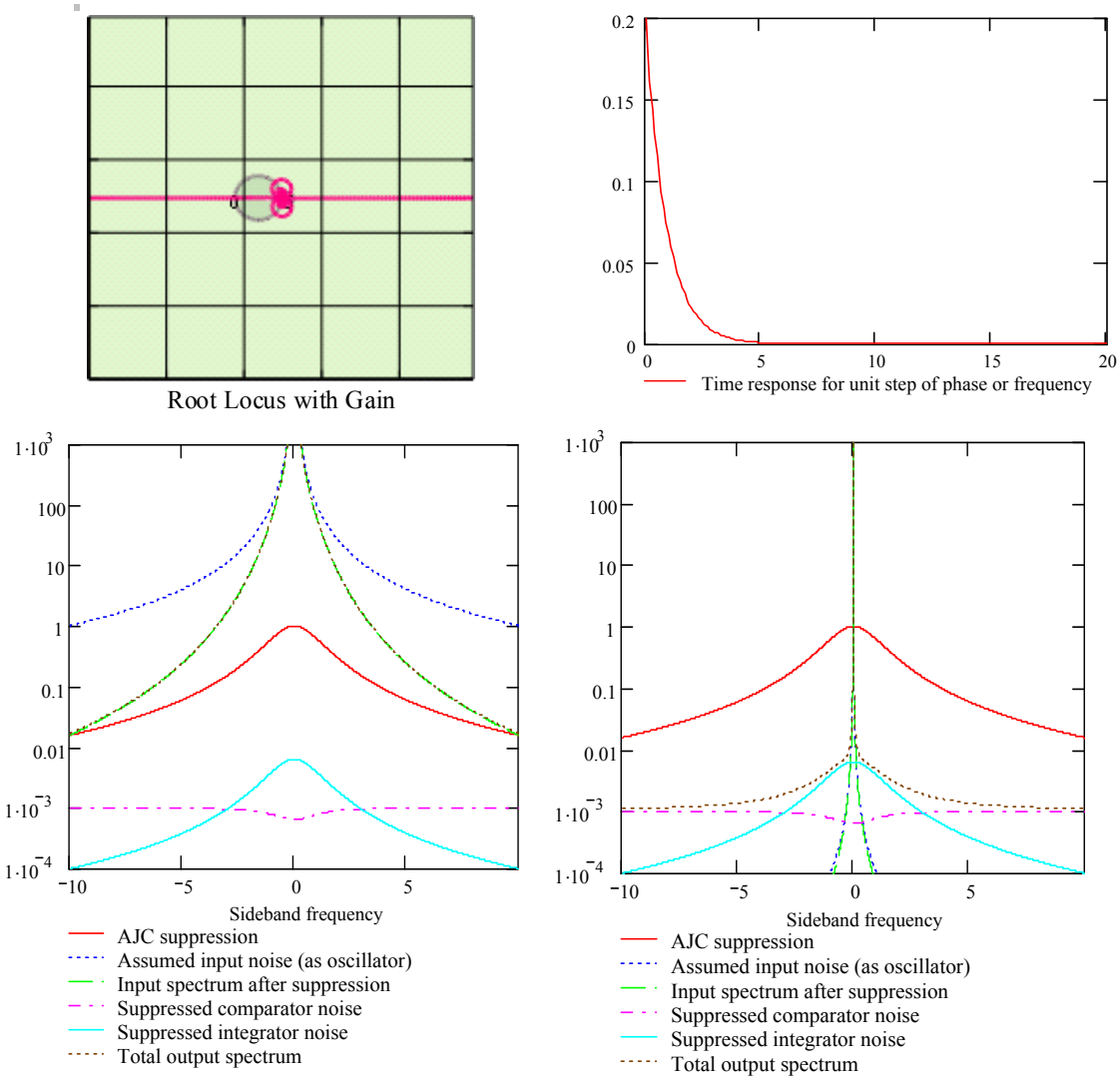

Fig. 8. Simple first order loop A2S2 plots -

Simple first order loop

The loop transfer function is has a single pole, which is the integrator time constant, and no zeroes. Actually there has to be at least one more pole coming from whatever type of dc feedback is being used, but this or any other poles are assumed to be at higher frequencies where they have minimal impact on control loop behaviour. In this example the normalised loop gain is k= 0.24.

Note that the suppression improves at a 6dB per octave rate and the close-in comparator noise is marginally improved.

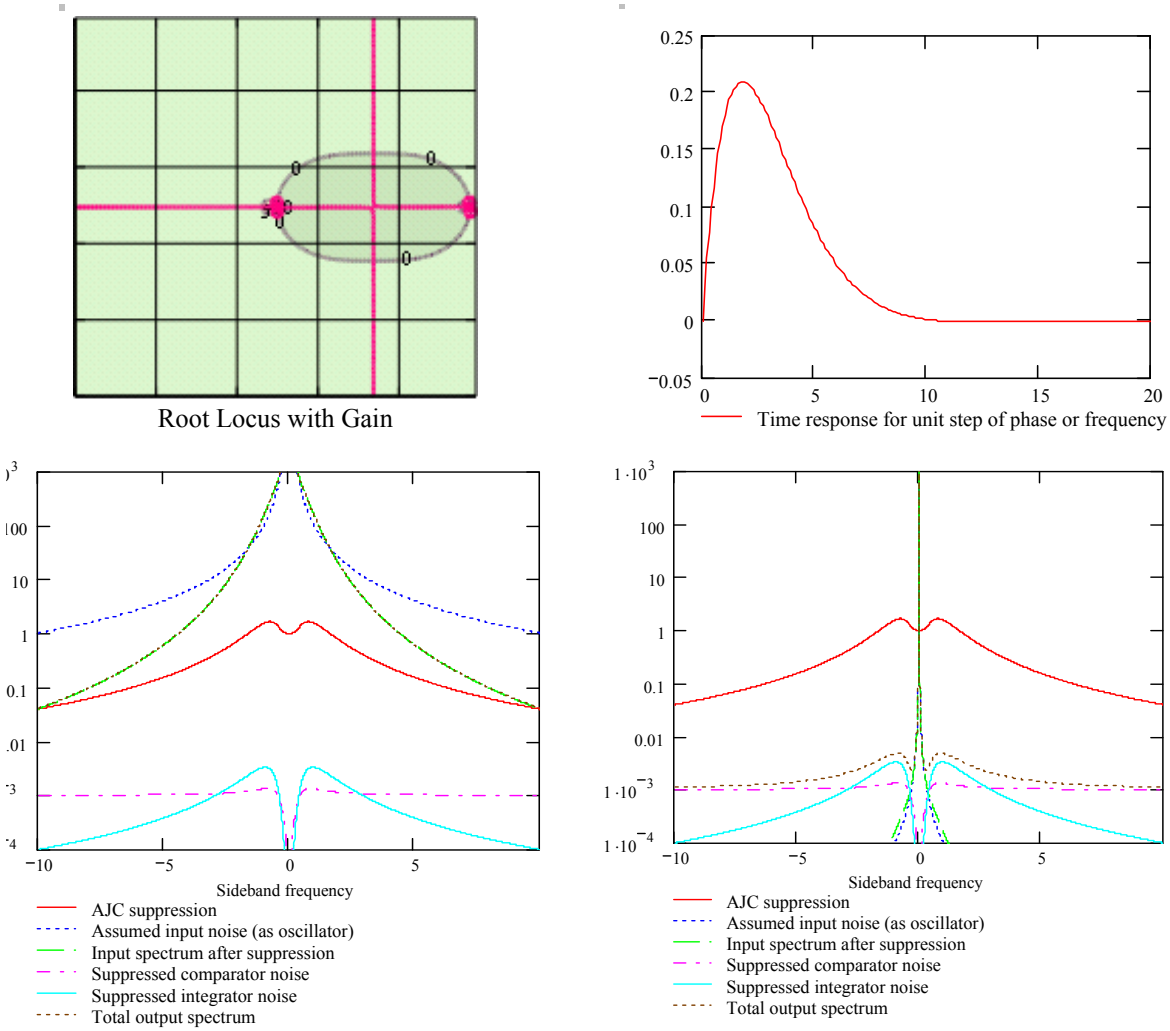

Fig. 9. Simple second order loop A2S2 plots -

Simple Second Order Loop

The simple second order loop example has two poles and no zeros. The pole frequencies are s = -1 and s = -0.05 with a 20:1 ratio between them. The loop gain k = 6.1. slightly underdamped

In this system the close-in internal or intrinsic noise is substantially suppressed and improved. This type of noise is progressively reduced (at +6dB / octave) to a limit of -40 dB as the carrier is approached.

The AJC suppression climbs at -12dB / octave towards a value of 0dB at the loop cut-off frequency. For critical damping, the AJC suppression turns into a very small amplification around the loop cut-off frequency. A badly under-damped system can make this amplification excessive for a narrow band of frequencies.

Note that a small amount of 'peaking' of the noise amplitude response does not much affect the total jitter; because as the amplitude gets greater, the bandwidth of the peaking gets proportionately smaller. The effect on the total jitter is therefore proportional to the square root of the noise peaking.

Note a considerably faster time response than for the previous system.

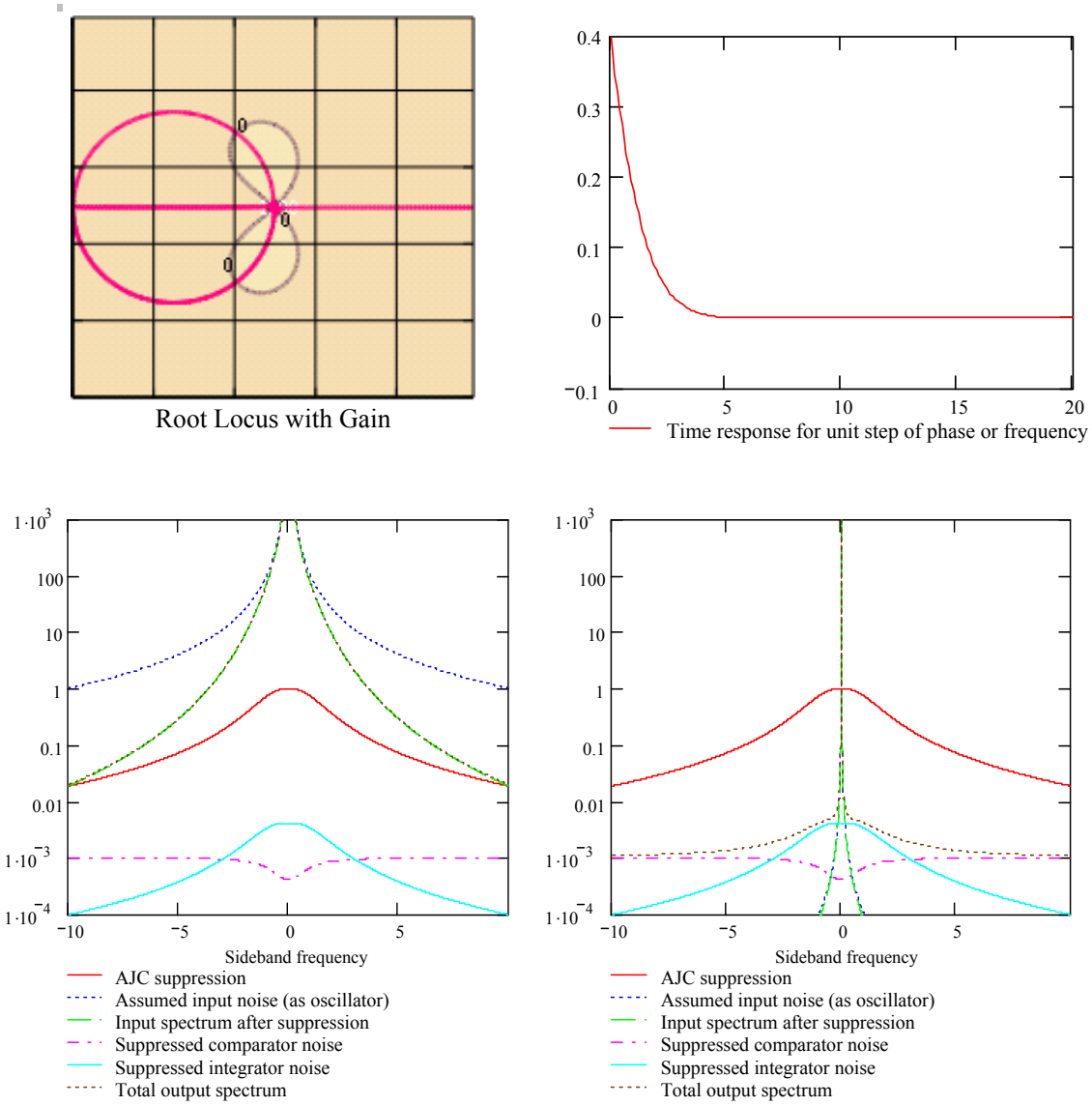

Fig. 10. Second Order Loop with LHP zero, A2S2 plots

Second Order Loop with LHP zero

The LHP (Left hand plane) zero can usefully be placed somewhere between 2.0 and 0.5 for a pair of poles at s = -1 The zero has the useful effect of decreasing the DC loop gain if appropriately placed. If the zero has to be placed lower than the integrator pole, it may require a large value capacitor that cannot easily be implemented on a chip.

But the example shown is for ac coupling which automatically introduces a zero with a pole. The zero is at 1.5 and the gain is k=0.56. The presence of a zero means that the ultimate suppression of this second order system is only approached at a -6dB / octave rate.

Note that time response is

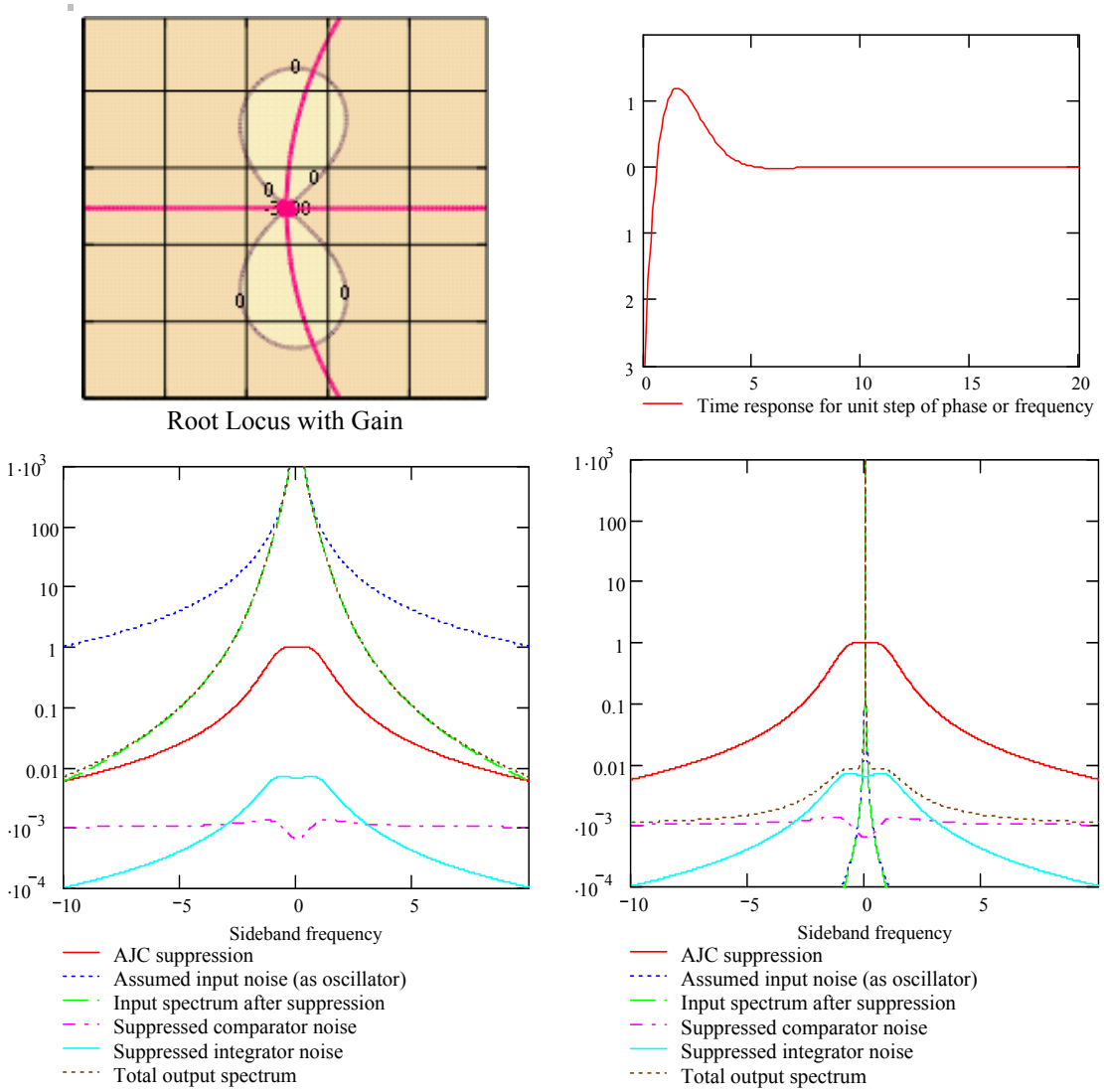

Fig. 11. Second order RHP zero, A2S2 plots

Second order RHP zero

If positive AC feedback is used with negative (DC) feedback, it is possible to place a zero in the RHP (right hand plane) of the AJC root locus. Such a pole can be used to reduce DC gain. and it can also be used to move a system pole to lower than its original frequency. The A^2S^2 plots (for k= 0.24) show a suppression at the loop corner frequency as good as -10 dB with a -6 dB/octave characteristic on both sides of this frequency.

Positive AC feedback can also be used to lower the zero suppression corner frequency to be up to ten times less than the integrator pole. It is important to note that the intrinsic noise corner frequency remains at the integrator pole frequency. With this method, the integrator pole frequency can then be allowed to rise, retaining much the same suppression characteristic but, theoretically with improved UI noise because the noise-peaking frequency has been increased to a point where the intrinsic noise is lower.

In spite of the lower effective pole frequency, the time response is still reasonably good but with some overshoot.

VI. AJC MEASUREMENTS

Fig. 12 shows an example of a discrete component AJC circuit as used for the results given in this paper.

Figs. 13 and 14 show typical suppression and intrinsic noise results at 40 MHz for such a discrete component AJC.

The reason for the asymmetry in the suppression frequency characteristic is not fully understood, but it is believed to be associated with unwanted RF coupling from

input to output at some point inside the circuit. Note that good suppression is obtained in spite of this.

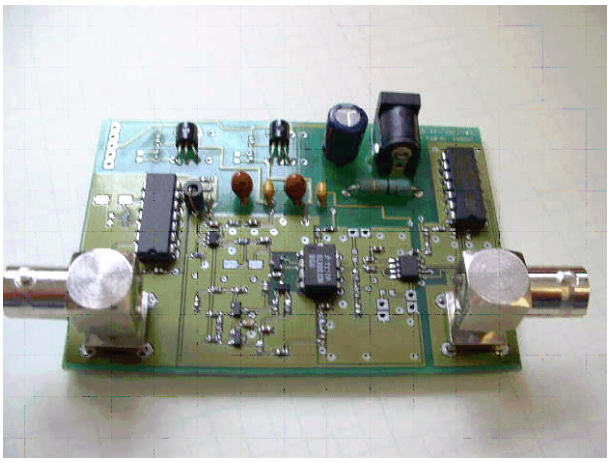

Fig. 12 Example discrete component AJC circuit

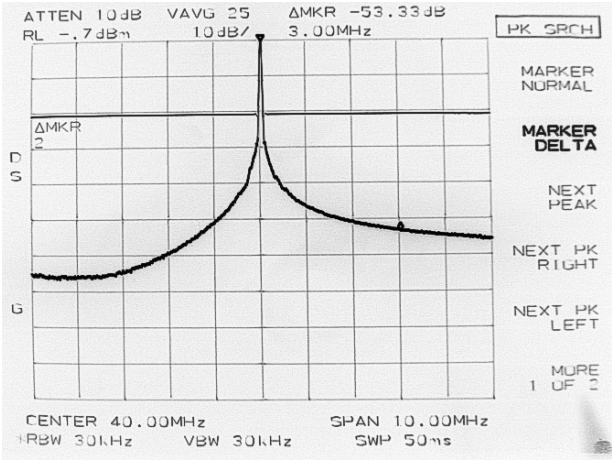

Fig. 13. AJC suppression at 40MHz

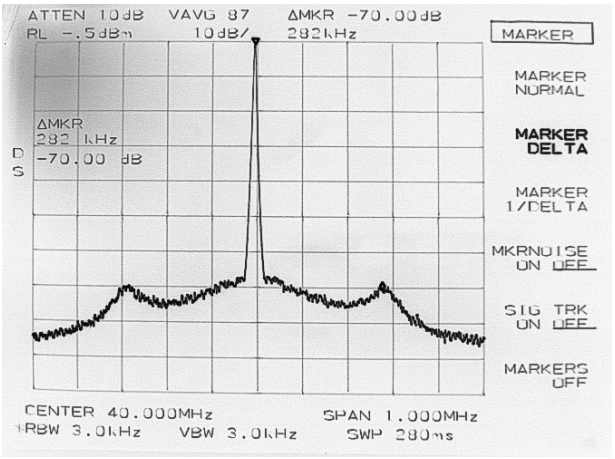

Fig. 14. AJC intrinsic noise at 40MHz

VII. FINDINGS AND CONCLUSIONS

The A2S2 Analytic AJC Systems Simulator is a useful tool for predicting the performance of an AJC design in respect of the frequency characteristics of suppression and the 'intrinsic' (internally generated) AJC noise. Good agreement is achieved between measurements and simulated results.

We find both from the simulator and from measurements that the AJC close-to-carrier noise (inside the loop bandwidth) is much less than for a typical PLL of the same bandwidth. For an AJC (discharge) current of 1mA the further out sideband noise corresponds to a VCO with a Q of about 5 to 10; with an increase of equivalent Q to 50 to 100 if the discharge current is raised to 10mA. These results are about 20dB worse than the theoretical predictions.

A comparator noise level of 1 to 10 nV/Hz and a sawtooth of 1V p-p gives a theoretical output noise level of -170 to -150 dBC.

A reason for the better than expected noise results is thought to be the relatively high 1v p-p sawtooth waveform on the capacitor together with the low kHz integrator pole frequency that can now be achieved.

Suppression of 20 to 40 dB per discrete component AJC is now reliably achievable. Limiting jitter has been measured at about 30ps or less typically at 40MHz.

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